

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Bert M. VERMEIRE et al.

Serial No.:

Filing Date: November 19, 2003

Examiner: Unknown

Group Art Unit: Unknown

For: **PROGNOSTIC CELL FOR
PREDICTING FAILURE OF
INTEGRATED CIRCUITS**

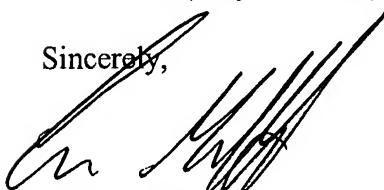
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P.O. Box 1450
Alexandria, VA 22313-1450

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Sincerely,



Eric A. Gifford
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<i>(Use as many sheets as necessary)</i>					
Sheet	1	of	2	Attorney Docket Number	300-01-1-001

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
	1	V. C. TYREE, "Self stressing test structure cells", Rome Laboratory, Air Force Materiel Command, February 1995, New York.		
	2	T. P. MA et al., "Ionizing Radiation Effects in MOS Devices and Circuits", John Wiley and Sons, 1989.		
	3	G. ANELLI et al., "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: Practical design aspects," IEEE Trans. Nucl. Sci., vol. 46, pp. 1690-1696, 1999.		
	4	G. S. SHARE, "Effects of Ionizing Radiation on Thin Oxide (20- 1500 Å) MOS Capacitors," J. Appl. Phys., vol. 45, pp. 4894, 1974.		
	5	R. C. LACOE et al., "Total-dose radiation tolerance of a commercial 0.35 mm CMOS process," presented at Radiation Effects Data Workshop, 1998.		
	6	R. C. LACOE et al., "Total-dose tolerance of a Chartered Semiconductor 0.35 mm CMOS process," presented at Radiation Effects Data Workshop, 1999.		
	7	R. C. LACOE et al., "Application of Hardness-By-Design Methodology to Radiation-Tolerant ASIC Technologies," IEEE Trans. Nucl. Sci., vol. 47, pp. 2334-2341, 2000.		
	8	R. C. LACOE et al., "Total-dose tolerance of the commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 mm CMOS process," presented at Radiation Effects Data Workshop, 2001.		
	9	J. W. R. DAWES et al., "Process technology for radiation-hardened CMOS integrated circuits," IEEE J. Solid State Circuits, vol. SC-11, pp. 459, 1976.		
	10	J.M. BENEDETTO et al., "Mosfet and MOS Capacitor Responses to Ionizing Radiation" IEEE Transactions on Nuclear Science, Vol. NS-31, No. 6, Decemebr 1984.		

Examiner Signature		Date Considered	
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INFORMATION DISCLOSURE
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Sheet

2

of

2

Application Number	
Filing Date	November 19, 2003
First Named Inventor	Bert M. VERMEIRE
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	300-01-1-001

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	11	A. MEKKAOUI et al., "30Mrad(SiO ₂) radiation tolerant pixel front end for the BTeV experiment," Nucl. Instr. and Meth. A, vol. 465, pp. 166-175, 2001.	
	12	J. D. M. FLEETWOOD, "A Reevaluation of Worst-Case Post-irradiation Response for Hardened MOS Transistors," IEEE Trans. Nucl. Sci., vol. NS-34, pp. 1178, 1987.	
	13	K. P. V. DRESSENDORFER, "The Effects of Test Conditions on MOS Radiation Hardness Results," IEEE Trans. Nucl. Sci., vol. NS-28, pp. 4281, 1981.	
	14	M. KIMURA, "Field and Temperature acceleration model for time-dependent dielectric breakdown," IEEE Trans. Electron Devices, vol. 46, pp. 220-229, 1999.	

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